SERIES ASYMMETRICAL HALF-BRIDGE CONVERTERS WITH VOLTAGE AUTO BALANCE FOR HIGH INPUT-VOLTAGE APPLICATIONS

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Abstract:

In this paper, an isolated Series Asymmetrical Half-Bridge Converters is proposed to satisfy the high power and high input-voltage requirements. In the proposed converter, two half-bridge modules with series configuration are adopted in the primary side to reduce the switch voltage stress to half of the input voltage. Moreover, the series half-bridge cells share the same transformer and leakage inductance, which simplifies the circuit structure. Zero-voltage-switching transition is achieved for all the active switches. Furthermore, the voltages of the input capacitors are automatically balanced without any additional components or complex control methods. In addition, a family of DC–DC converters with series half-bridge structure is explored to give extensive applications of the proposed contributions for the high input-voltage system.

Keywords: Asymmetrical half bridge converter, Pulse width modulation, Zero current resonant switch, Zero voltage resonant switch.

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I. INTRODUCTION

In recent years, the high-performance DC–DC converters have been called for the increasing high-voltage applications, such as the three-phase power factor correction (PFC) systems. However, the conventional full-bridge DC–DC converters are not suitable in these applications, due to the lack of commercial high-voltage high-performance power MOSFETs. For instance, in a three-phase PFC system with a 380 or 440 V_{ac} line voltage, only insulated-gate bipolar transistors (IGBTs) or few high-voltage MOSFETs can be used for the second-stage conventional DC-DC converter. This limits the switching frequency of the converter and impacts the power density improvement. In addition, the use of IGBTs or high-voltage MOSFETs results in decreased system efficiency due to their large voltage drops or conduction resistance. In order to overcome these aforementioned problems, many researchers focus on the switch voltage stress reduction to make the low-voltage high-performance MOSFETs available in the high input-voltage systems.

To reduce the switching losses, many zero-voltage switching (ZVS) or zero-voltage zero-current switching schemes in TLCs are proposed by adding auxiliary circuits or by applying improved control methods. Moreover, LLC resonance control strategy is also applied to TLCs for further power efficiency improvement.

Zero-voltage-transition techniques use a resonant feature between parasitic components during turn-on and/or turn-off transitions of the switching period. Therefore, ZVS techniques are easier to understand, analyze, and design than load-resonant techniques. Due to its simple configuration and zero-voltage switching (ZVS) characteristic, an asymmetric PWM half-bridge converter is one of the most popular topologies using the Zero-voltage-transition technique. In addition, the ripple component of the output current due to an output inductor becomes small enough to be handled by an appropriate output capacitor. Besides, the input-series output-parallel (ISOP) configuration is also employed to derive advanced high-voltage DC–DC converters, which connect the converter modules in series in the input side to reduce the primary switch voltage stresses. However, additional control techniques are required to ensure the equal sharing of the input voltage and load current, due to the parameter difference in each operation module.

In view of the ISOP converters, a series asymmetrical half-bridge converter (SA-HBC) is proposed to offer a novel solution for the high-voltage high-power applications. The SA-HBC

topology consists of two series half-bridge modules and shares the same primary leakage inductance, transformer, and secondary rectifier circuit. There are several clear highlights in the SA-HBC circuit. First, the switch voltage stress is limited to half of the input voltage, similar to the TLCs and ISOPs, so that the low-voltage MOSFETs can be used to improve the converter performance. Second, the ZVS transition is achieved for all MOSFETs to reduce the switching losses. Last but the most important, the voltages across the input capacitors are automatically balanced without any additional components or complex control methods.

II. PROPOSED CONVERTER AND OPERATIONAL PRINCIPLE

Main Circuit Structure:

The proposed SA-HBC's topology is illustrated in Fig. 1. The high-voltage input side consists of two DC-link capacitors C_1 and C_2, four main switches S_1–S_4 with their body diodes and parallel capacitors C_{S1}–C_{S4}, two DC blocking capacitors C_{b1} and C_{b2}, one transformer, and its leakage inductance L_k .The low-voltage output side is connected to the center-tapped windings of the transformer along with two rectifier diodes Do1 and Do2 and output filters Lo ,Co . Other secondary rectifier configurations are also suitable for the proposed topology. In this paper, a full-wave rectification with balanced windings in the secondary side is considered for the proposed SA-HBC converter. The primary turns of the transformer are n1, and the turns of the secondary side are n2. For the asymmetrical converters, the output filter inductor ripple current could be smaller by utilizing the unbalanced windings in the secondary side.

The generation rule of the proposed SA-HBC is presented in Fig. 2. Two series asymmetrical half-bridges with two independent transforms are plotted in Fig. 2(a). The DC capacitor C_1, main switches S_1 and S_2, DC blocking capacitor C_{b1}, the transformer, and leakage inductance compose the top asymmetrical half-bridge cell, while C_2 ,S_3 ,S_4 ,C_{b2}, the transformer and leakage inductance compose the bottom asymmetrical half bridge cell. It is reasonable to make S_1 and S_3 have the same driving signals with the duty cycle D, while S_2 is driven complementarily with S_1 and S_4 is driven complementarily with S_3. Therefore, according to the operation principle of the asymmetrical half-bridge converters, the voltage across the DC blocking capacitor $_{Cb1}$ equals $D \cdot Vin /2$ once two DC capacitors share the same DC voltage. The voltage across C_{b2} is $(1-D) \cdot Vin /2$.

It can be calculated that the primary sides of the two transformers suffer the same voltage of $(1-D)\cdot V_{in}/2$ when S1 and S3 are ON and share the voltage of $D\cdot V_{in}/2$ when S_2 and S_3 are ON and share the voltage of $D\cdot V_{in}/2$ when S_2 and S_4 are ON. As a result, we replace these two independent transformers with one individual transformer which is shared by the two series half-bridge cells. With this innovative concept, the primary side of the proposed SA-HBC topology is re-configured in Fig. 2(b). The sharing of the transformer makes the circuit structure of the SA-HBC circuit simple. Another sign ifcant advantage of the SA-HBC circuit is that the main switches S1−S4 and the series-connected DC blocking capacitors C_{b1} and C_{b2} introduce a built-in switched capacitor circuit for the input capacitors, which can automatically, balance the voltage across the DC capacitors.

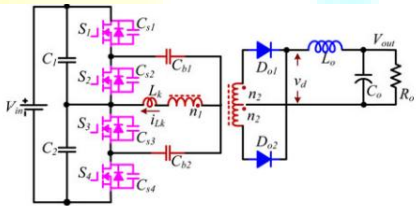


Fig. 1. Circuit of the SA-HBC.

Figure1: Circuit of SA-HBC

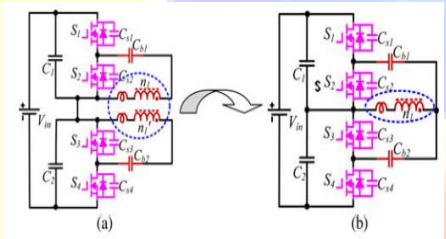


Fig. 2. Generation rule of the SA-HBC. (a) Series cells with independent transformers. (b) Proposed SA-HBC with a shared transformer.

Figure2: Generation rule of SA-HBC

Operation Analysis:

The driving signals of the proposed SA-HBC circuit are a little identical to the conventional asymmetrical half-bridge converter. The duty cycles of S_1 and S_3 are defined as D.

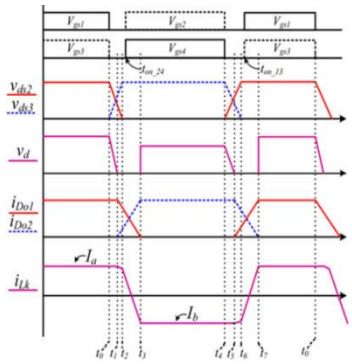


Figure3: Key waveforms of SA-HBC

In order to simplify the analysis of the SA-HBC, the following is assumed. The circuit operates in the steady state; the output voltage and current are constant with V_o and I_o; the DC blocking capacitors C_{b1} and C_{b2} have the same capacitance C_b and are large enough to ignore their voltage ripples; the magnetizing inductance of the transformer Lm is so large that the magnetizing current im is constant and ripple free; the parallel capacitors of MOSFETs C_{S1}–C_{S4} have the same capacitance C_s; the voltages across C_1 and C_2 are V_{in} /2; all devices are ideal. The key waveforms of the proposed SA-HBC converter are shown in Fig. 3.There are eight main stages in one switching period, and only four of them are analyzed in detail because the primary-side circuit is symmetrical. The equivalent circuit for each stage is illustrated in Fig. 4. Before t_0, SA-HBC works in the steady-state operation. Switches S1 and S3 are ON in the input side and diode D_{o1} is in the conduction state in the output side. The energy is transformed from the input side to the output side.

Stage 1 [t_0–t_1]:

At t_0, switches S_1 and S_3 begin to turn OFF. The current i_{Lk} remains unchanged with I_a. Thus, the capacitors C_{S1} and C_{S3} are charged linearly, while C_{S2} and C_{S4} are discharged. For the output side, V_d decreases in an approximately linear way and reaches zero at t1. V_d is given by

$$V_d(t)=[V_{ds2}(t)-V_{cb1}].n2/n1 \quad \ldots\ldots(1)$$

Stage 2 [t_1–t_2]:

In this stage, the voltage of the transformer keeps zero. For the input side, leakage inductance L_k begins to resonant with parallel capacitors C_{s1}–C_{s4}. The current i_{LK} flows through C_{S1} –C_{S4},

which charges C_{S1} and C_{S3} and discharges C_{S2} and C_{S4}. In the output side, diode D_{o2} begins to conduct. When the voltages of C_{S2} and C_{S4} reach zero at t_2 and C_{S1} and C_{S3} equal V_{in} /2, the ZVS transition for S_2 and S_4 is provided.

$$V_{LK}(t)=I_a Z_r.\sin\omega(t-t_1) \text{ .....(2)}$$

$$Z_r=\omega\sqrt{L_K/4C_S} \quad \omega=\sqrt{1/4C_S L_K} \text{ .....(3)}$$

Stage 3 [t_2 –t_3]: At t_2, the current i_{LK} flows through the anti-parallel diodes of S_2 and S_4. When S_2 and S_4 turn ON, ZVS turn-on transition is achieved. The voltage of the transformer still keeps zero and the voltage of the leakage inductance is clamped to V_{Cb1}. i_{LK} decreases linearly from I_a to I_b. In the output side, i_{Do1} decreases, while i_{Do2} increases linearly. When i_{Do1} reaches zero at t_3, the current i_{Lk} decreases to its minimum level I_b.

Stage 4 [t_3–t_4]:

During this stage, the SA-HBC works in S_2, S_4 ON operation period. The voltage of the leakage inductance keeps zero and its current i_{Lk} is the constant value of I_b. For the output side, only diode D_{o2} is ON and its current i_{Do2} keeps I_o. The voltage V_d is as follows:

$$V_d(t)=V_{cb1}.n_2/n_1 \text{ .....(4)}$$

The operation principles of Stages 5–8 are similar to those of Stages 1–4. In Stage 5, the output side voltage V_d is given in (5). In Stage 6, the resonant expression is shown in (6). In Stage 8 the SA-HBC works in static operation period; the voltage V_d is demonstrated in

$$V_d(t)=[V_{ds3}(t)-V_{cb2}].n2/n1 \text{ .....(5)}$$

$$V_{LK}(t)=I_b.Z_r.\sin\omega(t-t_5) \text{ .....(6)}$$

$$V_d(t)=V_{cb2}.n_2/n_1 \text{ .....(7)}$$

For all the operational stages, the voltages and currents of the DC blocking capacitors are given By $V_{Cb1}+ V_{Cb2}=V_{in}/2$ ….(8) , $i_{Cb1}+ i_{Cb2}=i_{Lk}/2$…(9)

III. CONVERTER PERFORMANCE ANALYSIS

The circuit performance of the proposed SA-HBC circuit is mainly concerned in four parts to help the electrical design. First, the circuit performance in ideal operation is investigated to provide a reference for the further analysis. Second, the output voltage of the SA-HBC is derived in detail considering the effect of leakage inductance. Third, the ZVS condition is explored to make sure that the SA-HBC can work with low switching losses. Last but not the least, the voltage auto balance principle of the SA-HBC is discussed theoretically to enhance the reliability of the proposed converter in high-voltage applications.

I*deal Operation Analysis:*

When ignoring the transition intervals, only Stage 4 and Stage 8 are investigated. By applying the voltage–second balance law to the leakage inductance L_k and magnetizing inductance L_m , the voltages across the DC blocking capacitors C_{b1} and C_{b2} can be calculated by

$V_{Cb1}=DV_{in}/2$, $V_{Cb2}=(1-D)V_{in}/2$

The current flowing through the magnetizing inductance Lm is constant and ripple free with the DC level I_m, since L_m is large enough. By applying the current–second balance law to the DC blocking capacitors C_{b1} and C_{b2}, the average current of the leakage inductance should be zero. In addition, the current values for I_m and i_{Lk} can be calculated by

$I_m=(1-2D).I_{0.}n_2/n_1$

$I_a=2(1-D).I_{0.}n_2/n_1$

$I_b= -2D.I_{0.}n_2/n_1$

Moreover, once ignoring the influence of the leakage inductance Lk and other parasitical parameter effects, the ideal output voltage can be calculated by $V_{out}=D(1-D).n_2/n_{1.}V_{in}$

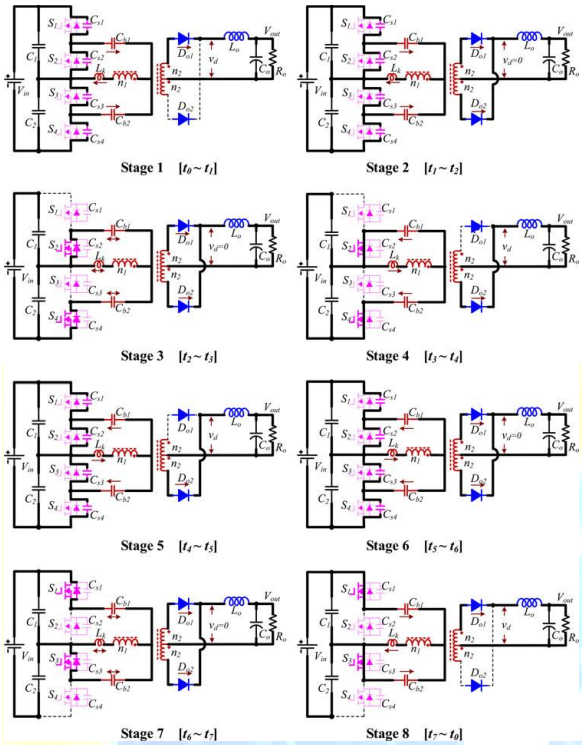


Figure4: Eight stages of proposed SA-HBC

Output voltage of SA-HBC:

The output voltage of SA-HBC is

$V_{out}=V_{Cb2}.n_2/n_1.(T_8+T_1/2)/T_s+V_{Cb2}.n_2/n_1.T4+T_5/T_8$

ZVS Transition:

To ensure the ZVS transition, two aspects should be considered. 1) The value of the characteristics impedance Z_r and 2)the dead time T_d between the driving signals.

$Z_r=\sqrt{L_k/4C_s}>=\max [D.V_{in}/(2.I_a),((1-D).V_{in})/-2.I_b]$

The dead time Td should satisfy

$\{T_d>\max(T_1+T_2,T_5+T_6)$

$\{T_{ib0}<\min(T_1+T_2+T_{ia0},T_5+T_6+T_{ib0})$

Voltage Auto-balance Principle:

Considering the proposed SA-HBC circuit without parasitic parameters, the current i_N that flows through the midline of the DC capacitors can be expressed as

i_N={$1/2i_{Cb1}$+$1/2i_{Cb2}$ stages 1,2,5 and 6

{i_{cb1} stages 3 and 4

{i_{cb2} stages 7 and 8

Pulse Width Modulation (PWM):

The energy that a switching power converter delivers to a motor is controlled by Pulse Width Modulated (PWM) signals, applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period. However, the width of the pulses changes from period to period according to a modulating signal.

When a PWM signal is applied to the gate of a power transistor, it causes the turn on and turns off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal. The frequency of a PWM signal must be much higher than that of the modulating signal, the fundamental frequency, such that the energy delivered to the motor and its load depends mostly on the modulating signal.

Symmetric PWM signals generate fewer harmonic in the output current and voltage. Different PWM techniques, or ways of determining the modulating signal and the switch-on/switch-off instants from the modulating signal, exist. The Technique that we use is Natural PWM technique. This technique is commonly used with three phase Voltage Source power inverters for the control of three-phase AC induction motors.

Hard switching and Soft Switching Techniques:

In the 1970's, conventional PWM power converters were operated in a switched mode operation. Power switches have to cut off the load current within the turn-on and turn-off times under the hard switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. During the turn-on and turn-off processes, the power device has to withstand

high voltage and current simultaneously, resulting in high switching losses and stress. Dissipative passive snubbers are usually added to the power circuits so that the dv/dt and di/dt of the power devices could be reduced, and the switching loss and stress be diverted to the passive snubber circuits. However, the switching loss is proportional to the switching frequency, thus limiting the maximum switching frequency of the power converters.

New generations of soft-switched converters that combine the advantages of conventional PWM converters and resonant converters have been developed. These soft-switched converters have switching waveforms similar to those of conventional PWM converters except that the rising and falling edges of the waveforms are 'smoothed' with no transient spikes. Unlike the resonant converters, new soft-switched converters usually utilize the resonance in a controlled manner. Resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS and ZCS conditions. Other than that, they behave just like conventional PWM converters. With simple modifications, many customized control integrated control circuits designed for conventional converters can be employed for soft-switched converters. Because the switching loss and stress have been reduced, soft-switched converter can be operated at the very high frequency (typically 500 kHz to a few Mega-Hertz). Soft-switching converters also provide an effective solution to suppress EMI and have been applied to DC-DC, AC-DC and DC-AC converters.

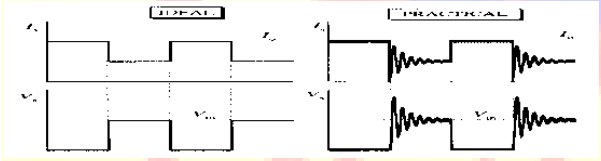


Figure5: Typical switching waveforms of (a) hard-switched and (b) soft-switched devices

Classification:

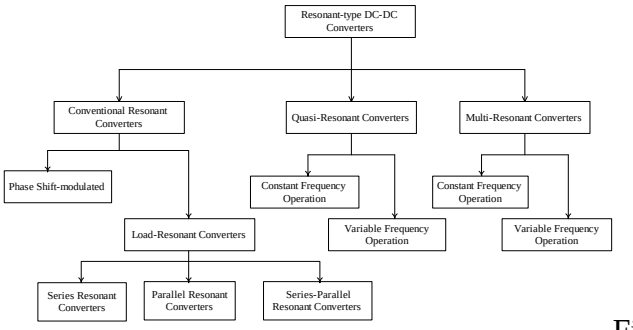


Figure6: Classification of Resonant Converters

Resonant Switch:

A resonant switch is a sub-circuit comprising a semiconductor switch *S* and resonant elements, L_r and C_r. The switch *S* can be implemented by a unidirectional or bidirectional switch, which determines the operation mode of the resonant switch. Two types of resonant switches, including zero-current (ZC) resonant switch and zero-voltage (ZV) resonant switches are shown in Fig.7 and Fig. 8 respectively.

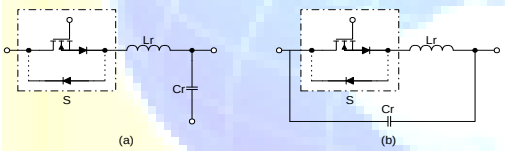


Figure7: Zero-current (ZC) resonant switch

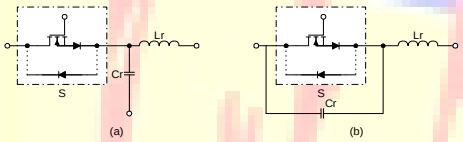


Figure8: Zero-voltage (ZV) resonant switch.

ZC resonant switch:

In a ZC resonant switch, an inductor L_r is connected in series with a power switch *S* in order to achieve zero-current-switching (ZCS). If the switch *S* is a unidirectional switch, the switch current is allowed to resonate in the positive half cycle only. The resonant switch is said to operate in *half-wave* mode. If a diode is connected in anti-parallel with the unidirectional switch, the switch current can flow in both directions. In this case, the resonant switch can operate in *full-wave* mode. At turn-on, the switch current will rise slowly from zero. It will then oscillate, because of the resonance between L_r and C_r. Finally, the switch can be commutated at the next

zero current duration. The objective of this type of switch is to shape the switch current waveform during conduction time in order to create a zero-current condition for the switch to turn off.

ZV resonant switch:

In a ZV resonant switch, a capacitor C_r is connected in parallel with the switch S for achieving zero-voltage-switching (ZVS). If the switch S is a unidirectional switch, the voltage across the capacitor C_r can oscillate freely in both positive and negative half-cycle. Thus, the resonant switch can operate in *full-wave* mode. If a diode is connected in anti-parallel with the unidirectional switch, the resonant capacitor voltage is clamped by the diode to zero during the negative half-cycle. The resonant switch will then operate in *half-wave* mode. The objective of a ZV switch is to use the resonant circuit to shape the switch voltage waveform during the off time in order to create a zero-voltage condition for the switch to turn on.

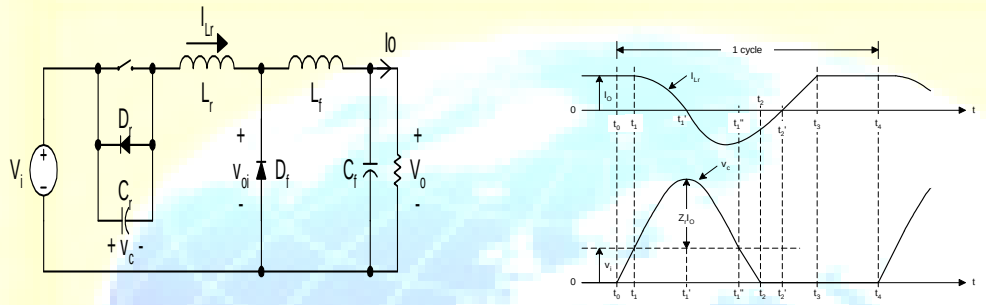
Quasi-resonant Converters:

Quasi-resonant converters (QRCs) can be considered as a hybrid of resonant and PWM converters. The underlying principle is to replace the power switch in PWM converters with the resonant switch. A large family of conventional converter circuits can be transformed into their resonant converter counterparts. The switch current and/or voltage waveforms are forced to oscillate in a quasi-sinusoidal manner, so that ZCS and/or ZVS can be achieved. Both ZCS-QRCs and ZVS-QRCs have *half-wave* and *full-wave* mode of operations.

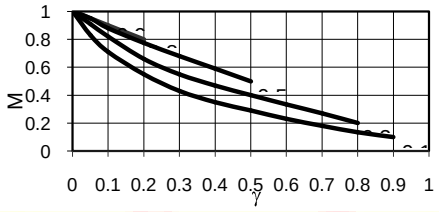
ZVS-QRC:

In these converters, the resonant capacitor provides a zero-voltage condition for the switch to turn on and off. A quasi-resonant buck converter designed for *half-wave* operation is shown in Fig.9 (a) - using a ZV resonant switch in Fig.9 (b). The steady-state circuit waveforms are shown in Fig.9 (b). Basic relations of ZVS-QRCs are given above. When the switch S is turned ON, the output current I_o passes through the line. The supply voltage V_i reverse-biases the diode D_f. When the switch is zero-voltage (ZV) turned off, the output current starts to flow through the resonant capacitor C_r. When the resonant capacitor voltage V_{Cr} is equal to V_i, D_f turns on. This starts the resonant stage. When V_{Cr} equals zero, the anti-parallel diode turns on. The resonant

capacitor is shorted and the source voltage is applied to the resonant inductor L_r. The resonant inductor current I_{Lr} increases linearly until it reaches I_o. Then D_f turns off. In order to achieve ZVS, S should be triggered during the time when the anti-parallel diode conducts. It can be seen from the waveforms that the peak amplitude of the resonant capacitor voltage should be greater or equal to the input voltage (i.e., $I_o Z_r > V_{in}$). From Fig.9(c), it can be seen that the voltage conversion ratio is load-sensitive. In order to regulate the output voltage for different loads r, the switching frequency should also be changed accordingly.



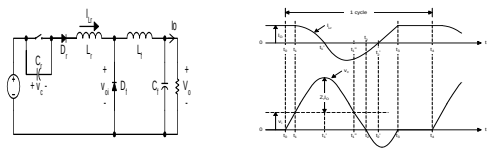
(a) Schematic diagram. (b) Circuit waveforms.



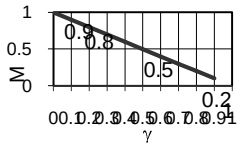
(c) Relationship between M and γ.

Figure9: Half-wave, quasi-resonant buck converter with ZVS.

ZVS converters can be operated in *full-wave* mode. The circuit schematic is shown in Fig.10 (a). The circuit waveforms in steady state are shown in Fig.10 (b). The relationships between M and γ at different r are shown in Fig.10.



(a) Schematic diagram. (b) Circuit waveforms.



(c) Relationship between *M* and γ.

Figure10: Full-wave, quasi-resonant buck converter with ZVS

It can be seen that *M* is load-insensitive in *full-wave* mode. This is a desirable feature. However, as the series diode limits the direction of the switch current, energy will be stored in the output capacitance of the switch and will dissipate in the switch during turn-on. Hence, the *full-wave* mode has the problem of capacitive turn-on loss, and is less practical in high frequency operation. In practice, ZVS-QRCs are usually operated in *half-wave* mode rather than *full-wave* mode.

Asymmetrical Half-Bridge Converters:

It provides complementary PWM control, where the high-side switch is driven ON for a duty cycle D and the low-side switch. The perfect option for this approach is an Asymmetrical Half Bridge converter it has high efficiency constant switching frequency operation and small output filter. Asymmetrical Half Bridge is a Perfect candidate for SD-SR because the transformer do not have dead times. Another main issue is its closed-loop controller does not be very fast, it will also cancel the previously shown low frequency ripple. A technique used to reduce the output voltage ripple is feed forward technique. Since LEDs is current driven devices in which light produced and the recombination of injected holes and electrons in a semiconductor junction, luminous intensity of LEDs are typically controlled by controlling the forward current only in one direction, another method for driving LEDs is using constant DC devices. The circuit comprises a pass-element (most often a power MOSFET), a sense element, a sense-signal conditioner, and a driver. The signal conditioner amplifies the sense signal and determines the polarity of the sensed voltage. When the applied voltage is of the correct polarity for forward conduction, the signal conditioner turns on the driver, which provides the necessary signal to operate the pass element. SR improves efficiency, thermal performance, power density, manufacturability, and reliability, and decreases the overall system cost of power supply systems. The two MOSFETs must be driven in a complimentary manner with a small dead time

between their conduction intervals to avoid shoot–through. The synchronous FET operates in the third quadrant, because the current flows from the source to the drain.

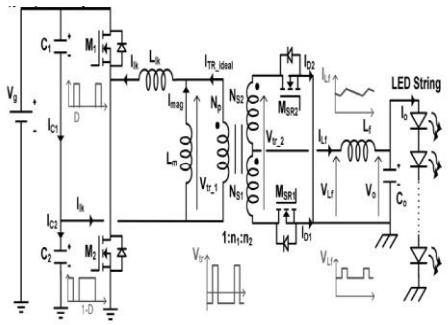


Fig. 1. Schematic Circuit Diagram of AHB

Figure11:Schematic of AHB

The schematic circuit diagram of the AHB is shown above in Fig. 11. It consists of an HB converter with their switches controlled with complementary signals. These complementarily driving signals imply that the voltages of the input capacitors are not necessarily equal signal.

Where V_{C1} and V_{C2} are the voltages across the input capacitor C_1 and C_2, D is the duty cycle and V_g is the input voltage of the AHB. The second important aspect regarding the AHB is the switching losses in MOSFETs and diodes. The switching losses of the MOSFETs can be reduced by employing the techniques that allow them to reach zero-voltage switching (ZVS). ZVS is quite difficult to achieve in the AHB because the amount of energy stored in the leakage inductance is not high enough. The asymmetric converter control was proposed to achieve ZVS operation for half bridge switches. Two drive signals are complementarily generated and applied to high-side and low-side switches respectively. The two HB switches may be turned on at ZVS conditions, attributing to the fact that the transformer primary current charges and discharges the junction capacitance. However, asymmetric stress distribution on the corresponding components may occur due to the asymmetric duty cycle distribution for the two primary switches. In other words, voltage and current stresses on the switches including both the primary side and secondary side MOSFETs are not identical. As a result, diodes or synchronous rectifiers with higher voltage rating are needed at the penalty of degrading the performance and efficiency of the rectifier stage.

AHB topology of on-board AC-DC converter for LED drivers is studied. The main points are summarized as below. This work focuses on the half-bridge converter due to its popularity, simplicity and adaptability for low voltage high-current applications. First, the half-bridge converter requires only two MOSFETs, which is only half of the number used in full-bridge topology. This helps to reduce the cost for practical applications. LEDs are slow loads; it is possible to design a feed-forward loop optimized for cancelling this low-frequency ripple, While the closed-loop control assures stability and output voltage regulation due to variations in the characteristics of the LEDs, which are determined by their warming-up. This AHB gives efficiency as 94.5%. For low voltage high current application this gives 12V voltage and 5A current for the corresponding input voltage.

The output waveforms for the proposed SA –HBC circuit can be seen in the following figures- Fig. 12, 13 and 14.

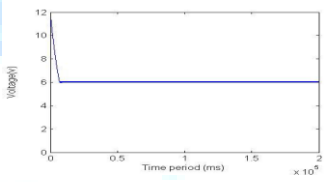
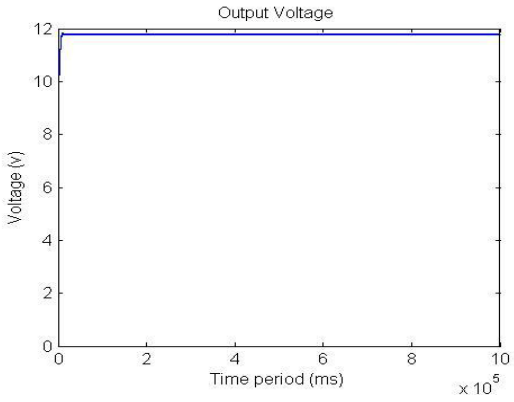


Figure12: Simulation Output for Open Loop



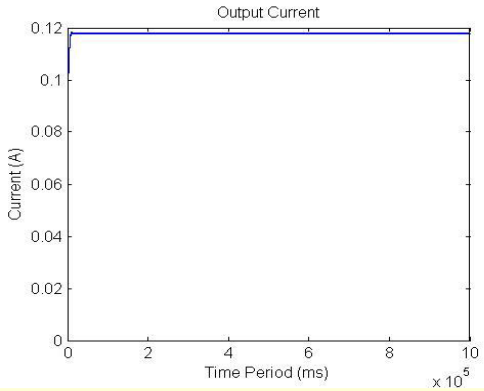


Figure13: Output voltage for V_g = 425V

Figure14: Output Current for Vg= 425V

CONCLUSION

A novel SA-HBC is introduced in this paper, providing a new solution for the high-voltage applications. By adopting series half-bridge configuration for the input side, the primary switch voltage stress is reduced to half of the input voltage. At the same time, ZVS soft switching transition is achieved by the leakage inductance to reduce the switching losses. Furthermore, the voltage auto balancing ability of the input capacitors is achieved, confirms the reliability of the converter for the high voltage applications. In addition, a family of DC-DC converters using the series half-bridge structure for high input-voltage application is discussed to expand the applications of the proposed circuit. At last, a 1 kW high-efficiency prototype converter with 500–600V input and 48V output is built to verify the analysis and the experimental results illustrate that the proposed converter is a competitive candidate for high-power and high voltage application.

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